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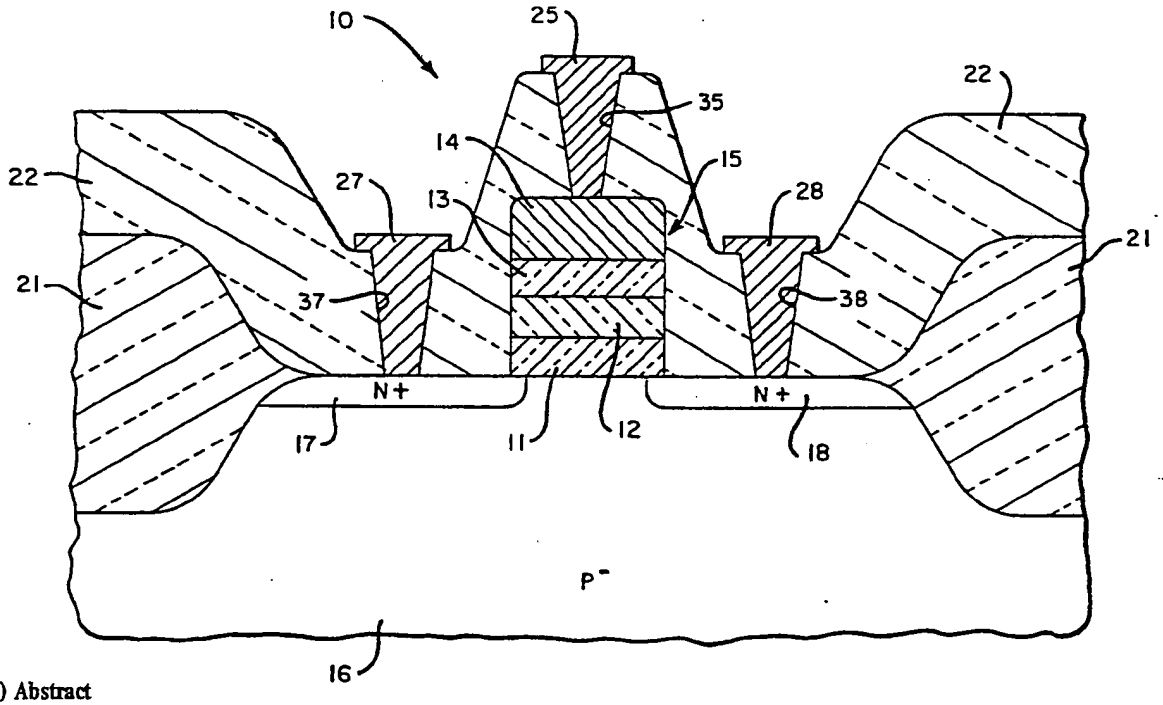

(57) Abstract

A non-volatile memory device includes a semiconductor substrate (16), a thin, 10-15 Angstroms thick, memory oxide layer (11), a silicon nitride layer (12), a 70-100 Angstroms thick interfacial oxide layer (13), and a polysilicon gate electrode (14). The interfacial oxide layer (13) is formed by chemical vapor deposition at a temperature in the range of about 600-625°C.

SILICON GATE NON-VOLATILE MEMORY DEVICE

Technical Field

This invention relates to non-volatile memory devices of the kind including a semiconductor substrate having provided thereon a first silicon dioxide layer, a silicon nitride layer provided on said first silicon dioxide layer and a silicon gate electrode overlying said silicon nitride layer.

The invention also relates to methods of making gate dielectric structures for non-volatile memory devices.

Background Art

Before discussing the background art, it is convenient to note the following four definitions of terms used in the present specification:

"SNOS" is silicon (polysilicon)-nitride-oxide-semiconductor.

"SONOS" is silicon (polysilicon)-oxide-nitride-oxide-semiconductor.

"Gate oxide" and "memory gate oxide" refer to the silicon dioxide dielectric formed between the semiconductor and the silicon nitride (SONOS) in the active area of a non-volatile memory device such as a capacitor or field-effect transistor.

"Interfacial oxide" refers to the silicon dioxide layer formed between the silicon gate and the silicon nitride dielectric in SONOS structures.

Two important characteristics of thin gate oxide, nitride non-volatile memory devices are retention and endurance. Retention is a measure of the ability of the memory device to retain its stored charge subsequent to a write or erase operation. Endurance is a measure of the retention of the memory device as a function of the number of write-erase cycles to which the device has been subjected.

A non-volatile memory device of the kind specified is known from an article by Peter C. Y. Chen entitled "Threshold-Alterable Silicon Gate MOS Devices", IEEE Transactions on Electron Devices, Vol. ED-24, No. 5, May, 1977.

Chen addresses the relatively poor retention of silicon gate structures: for example, a 15 Angstrom thick gate oxide provides retention measured in years in typical MNOS structures, but only in hours in SONOS structures. Chen increased the retention of his SONOS devices by increasing the thickness of the gate oxide to 30 Angstroms. However, increasing the oxide thickness has the disadvantage of slowing write and erase speeds.

Disclosure of the Invention

It is an object of the present invention to provide a non-volatile memory device of the kind specified having improved retention and endurance (or, equivalently, to reduce the rate of window closure of the memory window) without sacrificing performance characteristics such as write and erase speeds.

Therefore, according to the present invention, there is provided a non-volatile memory device of the kind specified, characterized by a second silicon dioxide layer located between said silicon nitride layer and said gate electrode and formed by chemical vapor deposition to a thickness of about 70-100 Angstroms, said first silicon dioxide layer having a thickness not greater than about 15 Angstroms.

It has been found that non-volatile memory devices according to the invention have good retention, endurance, and switching speed characteristics.

According to another aspect of the invention, there is provided a method of making a gate dielectric structure for a silicon gate non-volatile memory device, characterized by the steps of forming on a semiconductor

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SHEETS 1 & 2

Fig. 1

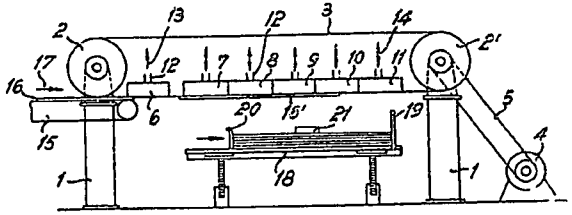


Fig. 2

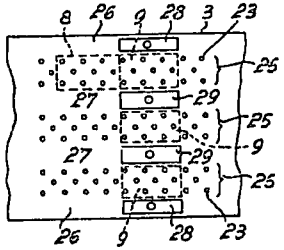


Fig. 3

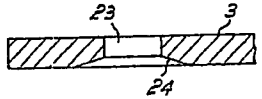


Fig. 4

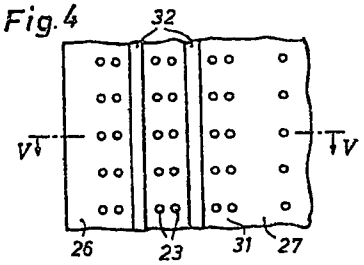


Fig. 5

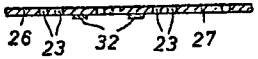


Fig. 6

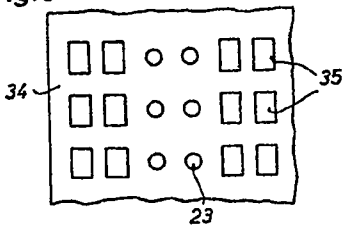
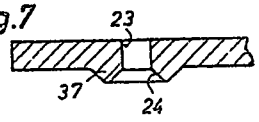


Fig. 7



substrate, a first, memory, silicon dioxide layer; forming on the first silicon dioxide layer a layer of silicon nitride; and forming on the silicon nitride layer a second, interfacial, silicon dioxide layer by chemical vapor deposition.

Brief Description of the Drawings

One embodiment of the invention will now be described by way of example with reference to the drawings, in which:

Fig. 1 is a cross-sectional representation of a silicon gate memory device embodying the principles of the present invention.

Fig. 2 is a graphical representation of the retention and endurance characteristics of prior art SNOS devices.

Fig. 3 is a graphical representation of the retention and endurance characteristics of SONOS devices embodying the characteristics of the present invention.

Best Mode for Carrying Out the Invention

A cross-section of an n-channel SONOS memory field effect transistor 10 embodying the features of the present invention is illustrated in Fig. 1. The device 10 is conventional except as noted. The illustrated device is formed by the well-known LOCOS (localized oxidation of silicon) process, although certainly the invention is not limited to this process. A p^- silicon substrate 16 has source- and drain-forming, opposite conductivity n^+ diffusions 17 and 18 therein, and a gate structure 15 which embodies the present invention. That is, the gate structure includes a very thin (about 10-15 Angstroms) gate oxide 11, a silicon nitride gate dielectric layer 12 of about 350 to 550 Angstroms thickness, an interfacial silicon dioxide gate dielectric layer 13 which is about 70-100 Angstroms thick, and a polysilicon gate electrode 14

which is typically several thousand Angstroms thick. Electrical contact is made to the source- and drain-forming diffusion 17 and 18 by electrodes 27 and 28, and to the silicon gate 14 by electrode 25. Also, electrical isolation of the device 10 is provided by field oxide layer 21 and isolation oxide layer 22.

The device 10 features the 70-100 Angstrom thick interfacial oxide layer 13 interposed at the nitride 12-polysilicon gate 14 interface and the very thin, 10-15 Angstroms thick, gate silicon oxide layer 11.

Typically, in forming the n-channel SONOS structure 10, the source 17 and drain 18 are formed by n-type impurities such as phosphorus (or p-type such as boron for p-channel) using diffusion or ion implantation techniques. The field oxide 21 can be formed by wet thermal oxidation of the substrate 16, to a typical thickness of 14K to 16K (14,000 to 16,000) Angstroms, as grown. The memory gate oxide 11 is preferably formed by dry thermal oxidation (thermal oxidation using dry oxygen), typically at 600 to 750°C. in an oxygen-nitrogen ambient. The memory nitride layer 12 can be deposited by the chemical vapor deposition technique at a temperature of about 700-750°C. using an ammonia-silane-nitrogen ambient. The interfacial oxide 13 is deposited by the atmospheric pressure chemical vapor deposition (APCVD) technique using a dry oxygen-silane-nitrogen ambient and a temperature of approximately 600°C, for example a temperature in the range of about 600-625°C. The polysilicon gate 14 can be formed using either the low pressure chemical vapor deposition (LPCVD) technique or the APCVD technique in an ambient of silane or silane-nitrogen, respectively, over the temperature range 600-700°C. Although the isolation oxide 22 can be formed by several techniques, the illustrated oxide is an APCVD oxide deposited at a temperature of about

425°C. in a silane-nitrogen-oxygen ambient to a typical thickness of about 6K Angstroms. Contacts 25, 27 and 28 are conductors such as aluminum or aluminum-silicon alloy which are formed using standard metallization techniques.

As mentioned, the silicon nitride gate dielectric layer 12 is preferably formed by chemical vapor deposition by reacting ammonia and silane (the nitrogen is a carrier gas) in a reactor maintained at 700-750°C. In order to prevent degradation of the gate structure 15 and, particularly, the silicon nitride 12 and to thereby avoid degrading the retention and endurance characteristics of the device, it is important to keep the temperature of post-nitride deposition processing to a minimum and preferably, below the nitride deposition temperature. The present embodiment achieves this purpose by forming the interfacial oxide layer 13 using the above-described low temperature APCVD technique. It should also be possible to generate the interfacial oxide layer 13 by other low temperature methods, for example, by the LPCVD technique.

Examples

The retention and endurance characteristics of SONOS devices embodying the characteristics of the present invention were compared with SNOS devices lacking those characteristics. Referring again to Fig. 1, both types of devices comprised n-channel silicon gate field-effect transistors. The SNOS devices were identical to the SONOS transistors 10 except that the SNOS devices lacked the interfacial oxide layer 13. The transistors were formed in accordance with the exemplary procedure described above. The substrate 16 was <100> p-type, 15-20 ohm-cm silicon. The final thickness of the field oxide 21 was 9K Angstroms; of isolation oxide 22, 6K Angstroms.

The gate structure 15 included 15 Angstroms thick gate memory oxide 11; 400-500 Angstroms thick gate memory nitride 12; 70 Angstroms thick APCVD interfacial oxide 13 (for the SONOS FETs only, not the SNOS FETs); and 3500 Angstroms thick APCVD polysilicon gate 14. The metallization was approximately 14K Angstroms aluminum.

The retention-endurance data of Figs. 2, 3 was obtained by (1) initializing the FETs by determining the initial written (or "1") and erased (or "0") threshold voltages V_T; (2) generating uncycled retention-endurance curves by storing the devices at an elevated temperature for the times shown in Figs. 2, 3 and determining the threshold voltages at intervals during this time; (3) write-erase cycling the FETs 10^4 times; (4) reinitializing the FETs; (5) generating retention-endurance curves for the 10^4 cycles by again storing at elevated temperature per step 2; (6) write-erase cycling to 10^5 total cycles; (7) reinitializing; and (8) generating retention-endurance curves for 10^5 cycles per step 2.

The initialization procedure (steps 1, 4 and 7), i.e. obtaining the initial written and erased state threshold voltages, involved applying +25 volts for three seconds and -25 volts for three seconds, respectively, at room temperature to the gates of the memory FETs. Source, drain and substrate were all tied to ground during this initialization.

Write-erase cycling (steps 3 and 6) was done at room temperature (approximately 24°C.) using an applied gate voltage of $\pm$25 volts and a 10 millisecond pulse width for both polarities. The source, drain and substrate were all tied to ground during the write-erase cycling.

The storage at temperature data for the uncycled and cycled parts (steps 2, 5 and 8) were obtained by first placing the parts in an oven at 125°C. in an air ambient to accelerate charge decay. (Note: The parts were packaged in metal cans to protect them

from mechanical damage and against potentially harmful exposure to the storage and room temperature ambients.) The parts were removed from the oven at various time intervals and the gate voltage required for a 20 micro-amp drain-source current (I_{DS}) was measured and recorded at room temperature. The decay of the stored charge, or equivalently, the rate of threshold voltage window closure as a function of log time for the SNOS and SONOS transistors, is shown in Figs. 2 and 3, respectively.

The main features of Figs. 2 and 3 are presented in Table I below.

TABLE I

Retention, Endurance Characteristics

FET Type	SNOS (Fig. 2)			SONOS (Fig. 3)		
Write-Erase Cycles	-	10^4	10^5	-	10^4	10^5
Window @ 1 hr, W_1 (Volts)	5.6	5.2	4.7	5.0	5.6	6.6
Window @ 10 hr, W_2 (Volts)	4.9	4.4	3.8	4.5	5.0	5.9
Window Decay Rate $\Delta W=(W_1-W_2)$/Decade (Volts/Decade)	0.7	0.8	0.9	0.5	0.6	0.7
Normalized Closure $\Delta W/W_1$	0.12	0.15	0.19	0.10	0.11	0.10

It should be noted that the initial threshold voltage window at 1 hour decreases with an increase in the number of write-erase cycles for the SNOS devices, while the window actually increases for the SONOS devices. Also, the normalized closure of the window between the "0" and "1" states threshold voltages increases significantly with increased write-erase cycles for the SNOS devices but changes very little for the SONOS devices. The SONOS devices, in addition, exhibit lower normalized decay rates (window closure) at all values of the write-erase cycles.

The addition of the interfacial oxide layer 13 (Fig. 1) and the resulting SONOS structure leads to a significant improvement in the normalized retention (window closure) and endurance characteristics of the basic SNOS memory structure. In fact, the window decay rates for the SONOS devices shown in Fig. 3 are close to that obtained by Chen in the above-referenced article, indicating that the 15 Angstrom-thick gate oxide samples provide the same retention as the thicker oxide SONOS structure required by Chen.

The improved normalized retention and endurance may in part be due to a reduction in the normalized charge leakage through the nitride to the polysilicon gate by virtue of the interfacial oxide layer which presents a potential barrier at this interface. However, the exact mechanism responsible for the improved normalized retention and endurance of the SONOS devices and for the increase in the voltage window with increased write-erase cycling is not understood.

Finally, it should be noted that the improved memory characteristics obtained with the monogate memory FET SONOS structure 10 should be equally valid for split-gate and trigate memory structures such as taught in U. S. 3,719,866 issued March 6, 1973 to Naber and Lockwood and assigned to NCR. Also, the improved memory characteristics are applicable to all

silicon gate structures to which the gate structure 15 is applicable, and includes capacitor structures (i.e. FET 10 without source 17 and drain 18) as well as transistor structures.

CLAIMS:

1. A non-volatile memory device including a semiconductor substrate (16) having provided thereon a first silicon dioxide layer (11), a silicon nitride layer (12) provided on said first silicon dioxide layer (11) and a silicon gate electrode (14) overlying said silicon nitride layer (12), characterized by a second silicon dioxide layer (13) located between said silicon nitride layer (12) and said gate electrode (14) formed by chemical vapor deposition to a thickness of about 70-100 Angstroms, said first silicon dioxide layer (11) having a thickness not greater than about 15 Angstroms.

2. A non-volatile memory device according to claim 1, characterized in that said first silicon dioxide layer (11) is about 10-15 Angstroms thick.

3. A non-volatile memory device according to claim 1, characterized in that said gate electrode (14) is formed of polysilicon.

4. A non-volatile memory device according to claim 1, characterized in that said second silicon dioxide layer (13) is a low temperature CVD layer (formed at about 600-625°C).

5. A non-volatile memory device according to any one of the preceding claims, characterized in that said device is a capacitor or a transistor.

6. A method of making a gate dielectric structure for a silicon gate non-volatile memory device, characterized by the steps of forming on a semiconductor substrate (16), a first, memory, silicon dioxide layer (11); forming on the first silicon dioxide layer (11) a layer of silicon nitride (12); and forming on the

6. (concluded)
silicon nitride layer (12) a second, interfacial, silicon dioxide layer (13) by chemical vapor deposition.

7. A method according to claim 6, characterized in that said first, memory, silicon dioxide layer (11) is formed to a thickness of about 10-15 Angstroms.

8. A method according to claim 7, characterized in that said step of forming a second, interfacial, silicon dioxide layer (13) by chemical vapor deposition is performed at a temperature of about 600-625°C.

9. A method according to claim 8, characterized in that said step of forming said second, interfacial, silicon dioxide layer (13) is effected by the reaction of silane and oxygen at atmospheric pressure.

10. A method according to claim 6, characterized in that said step of forming said first, memory, silicon dioxide layer (11) is effected by dry thermal oxidation at 600-750°C. in an oxygen-nitrogen ambient and in that said step of forming a layer of silicon nitride (12) is effected by chemical vapor deposition at 700-750°C. using an ambient of ammonia, silane and nitrogen.

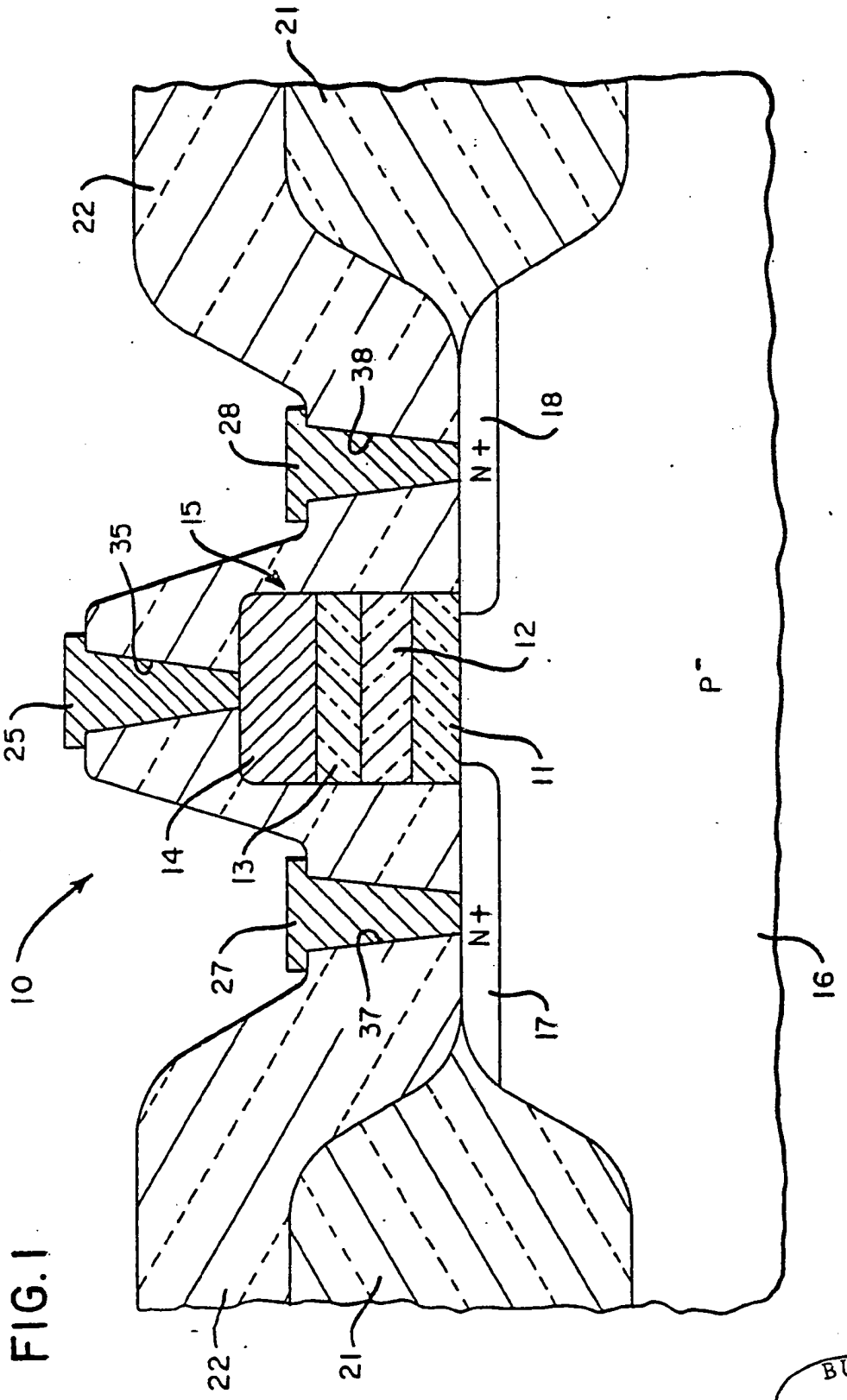


FIG. 1

FIG. 2
SNOS

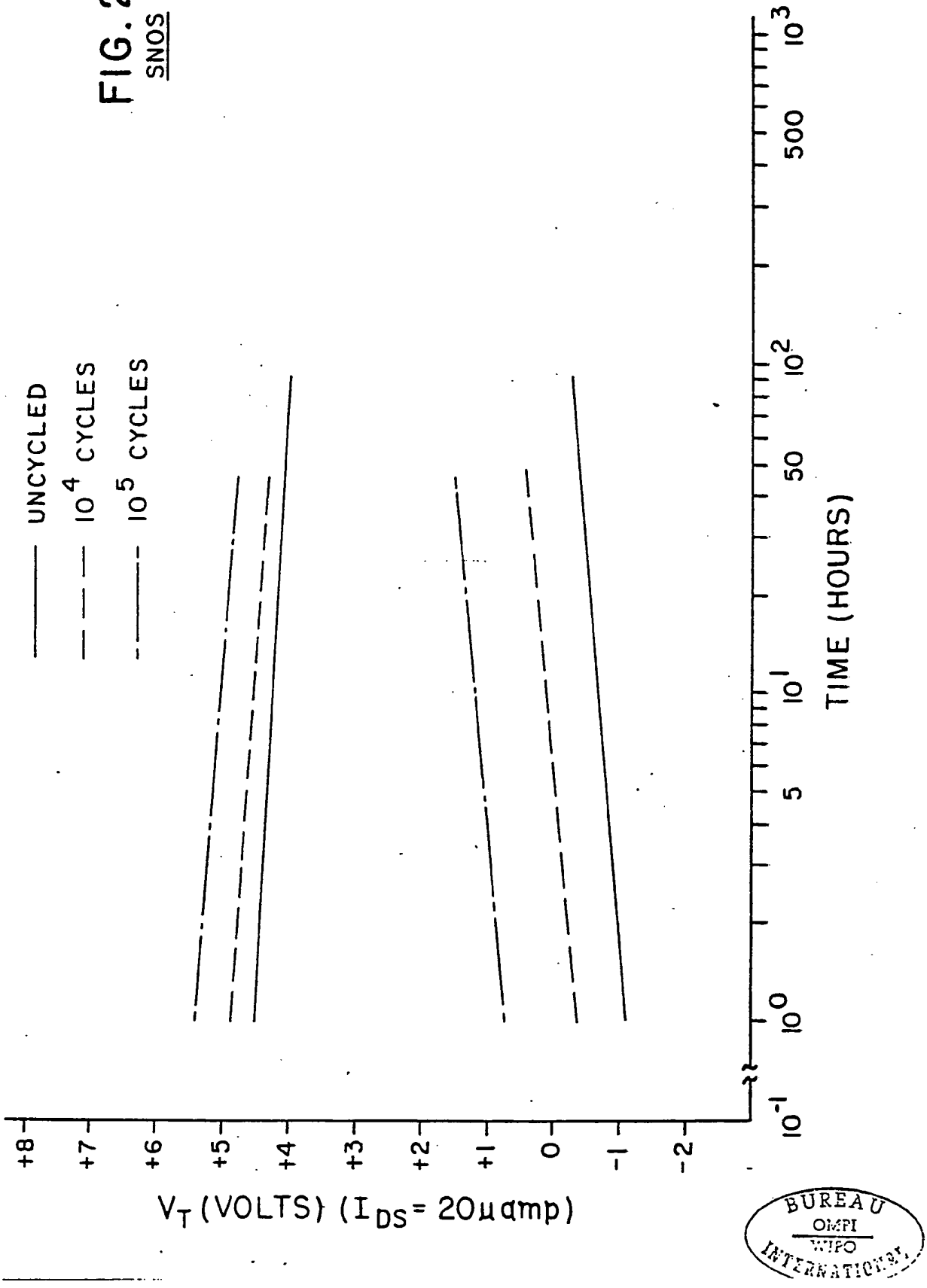
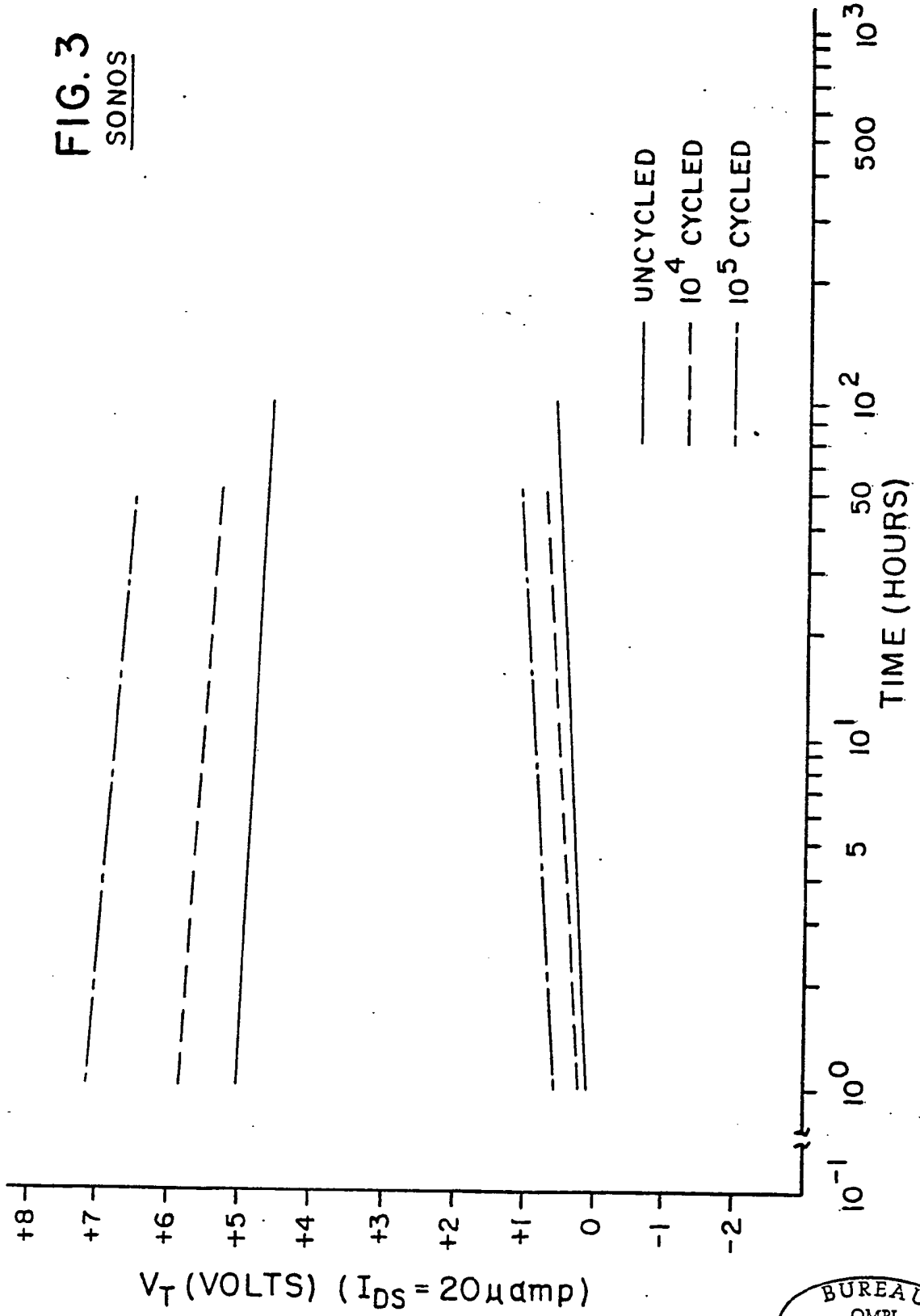


FIG. 3
SONOS



INTERNATIONAL SEARCH REPORT

International Application No PCT/US80/01179

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

INT. CL.: H01L 27/12,29/78,29/34,29/04; G11C 11/34

U.S. CL.: 357/4,23,54,59; 365/184

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
U.S.	357/4,23,54,59; 365/184

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
A	US, A, 4,151,021, PUBLISHED 24 APRIL 1979, McELROY	1-10
X	N, PROCEEDINGS OF THE IEEE, Volume 64 No. 7, ISSUED JULY 1976 (NEW YORK, NEW YORK), J. CHANG, "NON VOLATILE SEMICONDUCTOR MEMORY DEVICES," SEE FIGURE 20.	1-10
X	N, IBM TECHNICAL DISCLOSURE BULLETIN, Volume 18 No. 6, ISSUED NOVEMBER 1975 (ARMONK, NEW YORK), A. BHATTACHARYYA ET AL., "FET GATE STRUCTURE FOR NONVOLATILE N-CHANNEL READ-MOSTLY MEMORY DEVICE," PAGE 1768.	1-10
A	N, APPLIED PHYSICS LETTERS, Volume 31 No. 7, ISSUED OCTOBER 1977 (NEW YORK, NEW YORK) H. LEE, "A NEW APPROACH FOR THE FLOATING -GATE MOS NONVOLATILE MEMORY," PAGES 475, 476.	1-10

* Special categories of cited documents: [15]

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"X" document of particular relevance

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
22 OCTOBER 1980	05 FEB 1981
International Searching Authority [1]	**Signature of Authorized Officer** [20]
ISA/U.S.	Joseph E. Clawson Jr JOSEPH E. CLAWSON, JR.

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